

Appl. No. 10/001,271  
Amdt. dated August 28, 2003  
Reply to Office Action of June 3, 2003

### REMARKS/ARGUMENTS

Applicant respectfully requests Examiner's reconsideration of his rejections of the present application.

Claims 1 - 5 remain pending in the present application. Claims 6 - 10 have been withdrawn from further consideration as being drawn to non-elected subject matter.

Claims 1 - 5 are rejected under 35 U.S.C. §102(b), second paragraph, as being anticipated by *Dohya* (U.S. Patent No. 5,012,047).

#### The §102 rejection

*Dohya* as cited by the Examiner, "relates to a multilayer wiring substrate which includes a plurality of laminated wiring layers, a plurality of insulating layers for providing insulation between the wiring layers, and a plurality of hollows provided within at least one of the insulating layers (Abstract)." Furthermore, as the Office Action cites, "The layers 15 and 16 work as bonding pads for connecting leads of large scale 20 integrated circuits (LSI) circuits. . . (col. 2, lines 8-10)"

Applicant respectfully asserts that *Dohya* is applicable to **already packaged** IC devices. *Dohya* provides a printed circuit board at layers 15 and 16 the bonding pads required to connect the already-packaged IC device.

In contrast, Applicant's claimed invention provides a substrate for flip-chip packaging. The use of flip-chip packaging is relevant toward assembling device *die*

In addition the via holes 17 cited by *Dohya* (FIG. 1) are applicable to the manufacturing of printed circuit boards (PCB) capable of receiving already package IC devices. These *structurally different* holes have been defined with techniques useful in PCB manufacture in stark contrast with Applicant's claimed "*microvias* connecting said power bump pads. . . (claim 1)". *Dohya's* structural differences would render the multilayer wiring substrate incapable of performing its intended use if it were employed by Applicant's claimed invention, namely the making of optimum power and ground bump pad and bump patterns for flip-chip packaging.

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These microvias and the related technology could not have been anticipated by *Dohya*, given the change in the art of IC packaging at the time of *Dohya* (ca. 1991) versus Applicant's conception and filing (ca. 2001).

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Furthermore, MPEP §2131 provides:

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as contained in the . . . claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim.

Consequently, in that the elements of claim 1 are not all presented in *Dohya*, it cannot be a §102 reference. In light of the arguments presented, the §102 rejections are improper and should be withdrawn. Therefore, claim 1 is allowable and dependent claims 2 - 5 are also allowable (in that they depend upon an allowable base claim).

Applicant believes he has addressed the Examiner's concerns. Therefore, the claims are believed allowable over the cited reference. Applicant respectfully requests that a timely Notice of Allowance be issued in this case. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is encouraged to contact the undersigned at (408) 474-9063.

Please charge any fees other than the issue fee and credit any overpayments to Deposit Account 14-1270.

Respectfully submitted,

Date: 28-AUG-2003

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